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14. ABSTRACT
This progress report summarizes achievements in Professor Hochberg's research group at the University of Delaware in the development of three new application areas for silicon photonics. This work has been supported by the AFOSR PECASE award since February 2010.

The research goals including demonstrating radically new classes of nonlinear optical devices in the silicon system, demonstrating mid-infrared integrated optics in silicon and pursuing new investigations into using silicon resonators as high sensitivity biosensors will be discussed. The results of the research including scientific publications and patents are included in this report. AFOSR support has been acknowledged in all these publications and presentations.

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PECASE NEW DIRECTIONS FOR SILICON INTEGRATED OPTICS

Abstract
This progress report summarizes achievements in Professor Hochberg's research group at the University of Delaware in the development of three new application areas for silicon photonics. This work has been supported by the AFOSR PECASE award since February 2010. The group has now made a successful transition to U. Delaware, so this report summarizes the accomplishments at UW, and to date at UD.

The research goals began as a program centered on demonstrating radically new classes of nonlinear optical devices in the silicon system, demonstrating mid-infrared integrated optics in silicon and pursuing new investigations into using silicon resonators as high sensitivity biosensors. A considerable effort went into each of these areas, and in each case we were able to demonstrate results that advanced the state of the art for each device category, as described in the publications.

More recently, we have focused our efforts on developing novel devices within CMOS compatible silicon systems. In particular, we highlight two new results, both of which have significantly advanced the state of the art for silicon photonics: A novel high speed modulator and a high speed photodetector.

Over the coming two years, we intend to focus our efforts on improving the speed and voltage characteristics of silicon CMOS compatible devices, and on making a transition into integrated systems-on-chip. We've also begun a considerable effort on nonlinear characterization of RF photonic devices in silicon for applications in areas like radar, which are of great DOD interest.

The results of the research including scientific publications and patents are included in this report. AFOSR support has been acknowledged in all these publications and presentations.

Published Papers Associated with PECASE Support

1. M. Hochberg and T. Baehr-Jones, "Towards fabless silicon photonics," Nature Photonics 4, 492-494 (2010)
   Silicon photonic devices can be built using commercial CMOS chip fabrication facilities, or 'fabs'. However, nearly all research groups continue to design, build and test chips internally, rather than leveraging shared CMOS foundry infrastructure.

2. A. Spott, Y. Liu, T. Baehr-Jones, R. Ilic, and M. Hochberg, "Silicon Waveguides and Ring Resonators at 5," Applied Physics Letters 97, 213501 (2010)
   We demonstrate low loss ridge waveguides and the first ring resonators for the mid-infrared, for wavelengths ranging from 5.4 to 5.6 μm. Structures were fabricated using electron-beam lithography on the silicon-on-sapphire material system. Waveguide losses of 4.0±0.7 dB/cm are achieved, as well as Q-values of 3.0 k.

3. J.T. Kirk, G.E. Fridley, J.W. Chamberlain, E.D. Christensen, M. Hochberg, and D.M. Ratner, "Multiplexed inkjet functionalization of silicon photonic biosensors," Lab on a Chip, DOI: 10.1039/c0lc00313a (2011)
   The transformative potential of silicon photonics for chip-scale biosensing is limited primarily by the inability to selectively functionalize and exploit the extraordinary density of integrated optical devices on this platform. Silicon biosensors, such as the microring resonator, can be routinely fabricated to occupy a footprint of less than 50 x 50 mm; however, chemically addressing individual devices has proven to be a significant challenge due to their small size and alignment requirements. Herein, we describe a non-contact piezoelectric (inkjet) method for the rapid and efficient printing of bioactive proteins, glycoproteins and neoglycoconjugates onto a high-density silicon microring resonator biosensor array. This approach demonstrates the scalable fabrication of multiplexed silicon photonic biosensors for lab-on-a-chip applications, and is further applicable to the functionalization of any semiconductor-based biosensor chip.

4. M. Gould, T. Baehr-Jones, R. Ding, S. Huang, J. Luo, A.K.-Y. Jen, J-M Fedeli, M. Fournier, and M. Hochberg, "Silicon-polymer hybrid slot waveguide ring-resonator modulator," Optics Express 19, 3952-3961 (2011)
   We demonstrate a ring-resonator modulator based on a silicon-polymer hybrid slot waveguide

with a tunability of 12.7 pm/V at RF speeds and a bandwidth of 1 GHz, for optical wavelengths near 1550nm. Our slot waveguides were fabricated with 193 nm optical lithography, as opposed to the electron beam lithography used for previous results. The tunability is comparable to some of the best ringbased modulators making use of the plasma dispersion effect. The speed is likely limited only by resistance in the strip-loading section, and it should be possible to realize significant improvement with improved processing.

5. R. Ding, T. Baehr-Jones, W-J Kim, A. Spott, J-M Fedeli, S. Huang, J. Luo, A. K.-Y. Jen, L. Dalton, and M. Hochberg, "Sub-Volt Silicon-Organic Electrooptic Modulator," IEEE Journal of Lightwave Technology 29, 1112-1117 (2011)
Lowering the operating voltage of electrooptic modulators is desirable for a variety of applications, most notably in analog photonics and digital data communications. In particular for digital systems such as CPUs, it is desirable to develop modulators that are both temperature-insensitive and compatible with typically sub-2V CMOS electronics; however, drive voltages in silicon-based MZIs currently exceed 6.5V. Here we show an MZI modulator based on an electrooptic polymer-clad silicon slot waveguide, with a halfwave voltage of only 0.69V, and a bandwidth of 500 MHz.

6. A. Spott, T. Baehr-Jones, R. Ding, Y. Liu, R. Bojko, T. O'Malley, A. Pomerene, C. Hill, W. Reinhardt, and M. Hochberg, "Photolithographically fabricated low-loss asymmetric silicon slot waveguides," Optics Express 19, 10950-10958 (2011)
We demonstrate low-loss asymmetric slot waveguides in silicon-on-insulator (SOI). 130 and 180 nm wide slots were fabricated with a 248 nm stepper, in 200 nm thick silicon. An asymmetric waveguide design is shown to expand the range in which the TE0 mode is guided and suppress the TE1 mode, while still maintaining a sharp concentration of electric field in the center of the slot. Optical propagation losses of 2 dB/cm or less are shown for asymmetric slot waveguides with 130 nm wide slots and 320 and 100 nm wide arms.

7. R. Ding, T. Baehr-Jones, W-J Kim, B. Boyko, R. Bojko, A. Spott, A. Pomerene, C. Hill, W. Reinhardt, and M. Hochberg, "Low-loss asymmetric strip-loaded slot waveguides in silicon-on-insulator," Applied Physics Letters 98, 233303 (2011)
We report on low-loss asymmetric strip-loaded slot waveguides in silicon-on-insulator fabricated with 248 nm photolithography. Waveguide losses were 2 dB/cm or less at wavelengths near 1550 nm. A 40 nm strip-loading allows low-resistance electrical contact to be made to the two slot arms. The asymmetric design suppresses the TE1 mode while increasing the wavelength range for which the TE0 mode guides. This type of waveguide is suitable for building low insertion-loss, high-bandwidth, low drive-voltage modulators, when coated with an electro-optic polymer cladding.

8. Y. Liu, T. Baehr-Jones, J. Li, A. Pomerene and M. Hochberg, "Efficient Strip to strip-loaded slot mode converter in silicon-on-insulator," IEEE Photonics Technology Letters 23, 1496 (2011)
We present a mode converter in the silicon-on-insulator platform, which enables highly efficient, broadband coupling between a strip waveguide and a strip-loaded slot waveguide near 1.55 μm. The proposed converter has the benefit of electrically isolating the two arms of the slot waveguide. We fabricated and tested our mode converters, and achieved 0.81±0.49 dB per converter insertion loss in the best set of devices, in agreement with simulation.

9. R. J. Bojko, J. Li, L. He, T. Baehr-Jones, M. Hochberg, and Y. Aida, "Electron beam lithography writing strategies for low loss, high confinement silicon optical waveguides," Journal of Vacuum Science & Technology B 29, Issue 6 (2011)
The authors present a robust process for fabricating passive silicon photonic components by

direct-write electron beam lithography (EBL). Using waveguide transmission loss as a metric, we study the impact of EBL writing parameters on waveguide performance and writing time. As expected, write strategies that reduce sidewall roughness improve waveguide loss and yield. In particular, averaging techniques such as overlap or field shift writing reduce loss, however, the biggest improvement comes from writing using the smaller field-size option of our EBL system. The authors quantify the improvement for each variation and option, along with the tradeoff in writing time.

10. S. Huang, J. Luo, H-L Yip, A. Ayazi, X-H Zhou, M. Gould, A. Chen, T. Baehr-Jones, M. Hochberg, and A. K.-Y. Jen, "Efficient Poling of Electro-Optic Polymers in Thin Films and Silicon Slot Waveguides by Detachable Pyroelectric Crystals," Advanced Materials doi: 10.1002/adma.201102874 (2011)
The authors demonstrate that the electric field generated from pyroelectric crystals can be used to efficiently generate polar order in E-O polymers.

11. M. Gould, T. Baehr-Jones, R. Ding, and M. Hochberg, "Bandwidth enhancement of waveguide-coupled photodetectors with inductive gain peaking," Opt. Express 20, 7101-7111 (2012)
Here we propose leveraging the complexity available in silicon photonics processes to compensate for photodiode capacitance using a technique known as gain peaking. We predict that by simply including an inductor and capacitor in the photodetector circuit with the properly chosen values, detector bandwidths can be as much as doubled, with no undesired effects.

12. T. Baehr-Jones, R. Ding, Y. Liu, A. Ayazi, T. Pinguet, N. C. Harris, M. Streshinsky, P. Lee, Y. Zhang, A. E-J Lim, T-Y Liow, S. H-G Teo, G-Q Lo, and M. Hochberg, "Ultralow drive voltage silicon traveling-wave modulator," Opt. Express 20, 12014-12020 (2012)
We demonstrate operation of a traveling-wave modulator with a drive voltage of 0.63 Vpp at 20 Gb/s, a significant improvement in the state of the art, with an RF energy consumption of only 200 fJ/bit.

13. T. Baehr-Jones, R. Ding, A. Ayazi, T. Pinguet, M. Streshinsky, N. Harris, J. Li, L. He, M. Gould, Y. Zhang, A. E-J Lim, T-Y Liow, S. H-G Teo, G-Q Lo and M. Hochberg, "A 25 Gb/s Silicon Photonics Platform," arXiv:1203.0767v1
We demonstrate an optical-lithography, wafer-scale photonics platform with 25 Gb/s operation. We also demonstrate modulation with an ultra-low drive voltage of 1 Vpp at 25 Gb/s. We demonstrate attractive cross-wafer uniformity, and provide detailed information about the device geometry. Our platform is available to the community as part of a photonics shuttle service.

14. A. Ayazi, T. Baehr-Jones, Y. Liu, A. E-J Lim, and M. Hochberg, "Linearity of silicon ring modulators for analog optical links," Opt. Express 20, 13115-13122 (2012)
We study the nonlinear distortions of a silicon ring modulator based on the carrier depletion effect for analog links. Key sources of modulation nonlinearity are identified and modeled. We find that the most important source of nonlinearity is from the pn junction itself, as opposed to the nonlinear wavelength response of the ring modulator. Spurious free dynamic range for intermodulation distortion of as high as 84dB.Hz^(2/3) is obtained.

15. L. He, Y. He, A. Pomerene, C. Hill, S. Ocheltree, T. Baehr-Jones, M. Hochberg, "Ultra-thin Silicon-on-Insulator Grating Couplers," Photonics Technology Letters. Vol. 24, No. 24 (2012)
We demonstrate a novel grating coupler (GC) fabricated on a Silicon-on-Insulator (SOI) wafer operating at 1550 nm, based on an ultra-thin 50 nm silicon geometry. The devices were fabricated in a complementary-metal-oxide-semiconductor (CMOS)-compatible process with a single etch step. Low insertion loss of -3.7 dB is achieved. We also calculate the backreflection loss to be -

14 dB. The devices are likely to be useful in terms of light coupling between optical fibers and ultra-thin silicon waveguides.

16. M. Gould, A. Pomerene, C. Hill, S. Ocheltree, Y. Zhang, T. Baehr-Jones and M. Hochberg, "Ultra-thin silicon-on-insulator strip waveguides and mode couplers," Applied Physics Letters 101, 221106 (2012)
We demonstrate an ultra-thin silicon waveguide for wavelengths around 1.55 lm, and mode converters designed for transitions to and from standard 500 nm x 220 nm strip waveguides. The devices were fabricated in a CMOS-compatible process requiring two photolithography and etch steps. The ultra- thin waveguides exhibited losses of 2.01 +/- 0.231 dB/cm, exhibited bend radii as small as 30 lm with losses of 0.05 +/- 0.005 dB per bend, and exhibited coupling losses of 0.66 +/- 0.014 dB to standard strip waveguides.

17. N. C. Harris, T. Baehr-Jones, A. E-J Lim, T. Y. Liow, G. Q. Lo, M. Hochberg, "Noise characterization of a waveguide-coupled MSM photodetector exceeding unity quantum efficiency," Journal of Lightwave Technology, Vol. 31, No. 1 (2013)
In the field of silicon photonics, it has only recently become possible to build complex systems. As system power constraints and complexity increase, design margins will decrease—making understanding device noise performance and device-specific noise origins increasingly necessary. We demonstrate a waveguide-coupled germanium MSM photodetector exhibiting photoconductive gain with a responsivity of 1.76 A/W at 5V bias and 10.6fF±0.96fF capacitance. Our measurements indicate that a significant portion of the dark current is not associated with the generation of shot noise. The noise elbow at 5V bias is measured to be approximately 150MHz and the high frequency detector noise reaches the Johnson noise floor.

18. J. T. Kirk, N. D. Brault, T. Baehr-Jones, M. Hochberg, S. Jiang, D. M. Ratner, "Zwitterionic polymer-modified silicon microring resonators for label-free biosensing in undiluted human plasma," Biosensors and Bioelectronics 42 (2013)
A widely acknowledged goal in personalized medicine is to radically reduce the costs of highly parallelized, small fluid volume, point-of-care and home-based diagnostics. Recently, there has been a surge of interest in using complementary metal-oxide-semiconductor (CMOS)-compatible silicon photonic circuits for biosensing, with the promise of producing chip-scale integrated devices containing thousands of orthogonal sensors, at minimal cost on a per-chip basis. A central challenge in biosensor translation is to engineer devices that are both sensitive and specific to a target analyte within unprocessed biological fluids. Despite advances in the sensitivity of silicon photonic biosensors, poor biological specificity at the sensor surface remains a significant factor limiting assay performance in complex media (i.e. whole blood, plasma, serum) due to the non-specific adsorption of proteins and other biomolecules. Here, we chemically modify the surface of silicon microring resonator biosensors for the label-free detection of an analyte in undiluted human plasma. This work highlights the first application of a non-fouling zwitterionic surface coating to enable silicon photonic-based label-free detection of a protein analyte at clinically relevant sensitivities in undiluted human plasma.

19. Y. Zhang, S. Yang, A. E-J Lim, G-Q Lo, C. Galland, T. Baehr-Jones, and M. Hochberg, "A compact and low loss Y-junction for submicron silicon waveguide," Optics Express Vol. 21 No. 1 (2013)
We designed a compact, low-loss and wavelength insensitive Y- junction for submicron silicon waveguide using finite difference time- domain (FDTD) simulation and particle swarm optimization (PSO), and fabricated the device in a 248 nm complementary metal-oxide-semiconductor (CMOS) compatible process. Measured average insertion loss is 0.28 ± 0.02 dB, uniform across an 8-inch wafer. The device footprint is less than 1.2 μm x 2 μm, an order of

magnitude smaller than typical multimode interferometers (MMIs) and directional couplers.

20. M. Streshinsky, A. Ayazi, Z. Xuan, A. E-J Lim, G-Q Lo, T. Baehr-Jones, and M. Hochberg, "Highly linear silicon traveling wave Mach-Zehnder carrier depletion modulator based on differential drive," Optics Express Vol. 21 No. 3 (2013)
We present measurements of the nonlinear distortions of a traveling-wave silicon Mach-Zehnder modulator based on the carrier depletion effect. Spurious free dynamic range for second harmonic distortion of 82 dB·Hz1/2 is seen, and 97 dB·Hz2/3 is measured for intermodulation distortion. This measurement represents an improvement of 20 dB over the previous best result in silicon. We also show that the linearity of a silicon traveling wave Mach-Zehnder modulator can be improved by differentially driving it. These results suggest silicon may be a suitable platform for analog optical applications.

21. W. Shi, X. Wang, C. Lin, H. Yun, Y. Liu, T. Baehr-Jones, M. Hochberg, N. A. F. Jaeger, and L. Chrostowski, "Silicon photonic grating-assisted, contra-directional couplers," Optics Express Vol. 21 No. 3 (2013)
We demonstrate, in both theory and experiment, 4-port, electrically tunable photonic filters using silicon contra-directional couplers (contra-DCs) with uniform and phase-shifted waveguide Bragg gratings. Numerical analysis, including both intra- and inter-waveguide couplings, is performed using coupled-mode theory and the transfer-matrix method. The contra-DC devices were fabricated by a CMOS-photonics manufacturing foundry and are electrically tunable using free-carrier injection. A 4-port, grating-based photonic resonator has been obtained using the phase-shifted contra-DC, showing a resonant peak with a 3-dB bandwidth of 0.2 nm and an extinction ratio of 24 dB. These contra-DC devices enable on-chip integration of Bragg-grating-defined functions without using circulators and have great potential for applications such as wavelength-division multiplexing networks and optical signal processing.

22. Y. Zhang, S. Yang, A. E-J Lim, G-Q Lo, C. Galland, T. Baehr-Jones, and M. Hochberg," A CMOS-Compatible, Low-Loss, and Low-Crosstalk Silicon Waveguide Crossing," IEEE Photonics Technology Letters, Vol. 25, No. 5 (2013)
We demonstrated a waveguide crossing for submicron silicon wavegVuides with average insertion loss of 0.18 ± 0.03 dB and crosstalk of-41 ± 2 dB, uniform across 8-inch wafer. The device was fabricated in a CMOS-compatible process using 248 nm lithography, with only one patterning step.

Design and characterization of a 30GHz bandwidth low-voltage silicon traveling-wave modulator

We present the design and characterization of a differential-drive silicon PN junction traveling-wave Mach-Zehnder modulator near 1550nm wavelength. The device is 3mm long and shows 30GHz 3dB bandwidth at a low reverse bias voltage of 1V. Under such bias condition the $V_\pi L_\pi$ is 2.7V-cm and accordingly the small-signal V_π is 9V. The insertion loss on the phase shifter is 3.6dB ± 0.4dB. The device performance metrics in combination show significant improvement in the state of the art, enabling 40~60Gb/s operation with low drive voltage requirement and practical insertion loss. Critical design tradeoffs are analyzed and design models are validated with measurement results. Several key RF design issues in traveling-wave Mach-Zehnder modulators are addressed for the first time.

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1. Introduction

Silicon optical modulators [1] are critical for data communication related applications [2-5] in silicon photonics. Over the past decade, significant progress has been made in this area, but achieving efficient high-speed modulation in silicon still proves to be challenging, mainly due to the weak electro-optic (EO) effects available in this material [5].

The fundamental and key modulator device metrics include insertion loss, device bandwidth, and EO modulation efficiency (for Mach-Zehnder modulators the efficiency is characterized by V_π). In addition, optical bandwidth, device footprint, temperature sensitivity, fabrication error tolerance and CMOS compatibility are also of great importance for practical designs, design scalability and possibility of CMOS monolithic integration [7,8].

A majority of the high-speed demonstrations thus far have been based on reverse-biased silicon PN junctions. Among these results, high-speed resonator modulators are promising in achieving ultra-low modulation power consumption and compact device footprint. Recently, Li et al demonstrated a 40Gb/s 1V-drive ring modulator [9], although a few issues remain to be fully addressed, such as limited optical bandwidth, and consequently necessary thermal drift stabilization as well as operating wavelength alignment between devices.

The other main category of carrier-depletion PN junction modulators is traveling-wave Mach-Zehnder (TWMZ) modulators. Although in academic demonstrations imbalanced Mach-Zehnder (MZ) modulators are often used (mostly for the convenience of testing), balanced MZ modulators are the true practical devices and have the key advantage of being temperature insensitive, thus do not require active thermal stabilization. Traveling-wave design enables the driving of a long phase-shifter at high speed, therefore can yield low voltage modulators.

40~60Gb/s channel speed is a logical next step from existing 25~28Gb/s data rates. The device we present here targets at applications at these speeds or equivalently a device bandwidth of approximately 30GHz [9-11]. In recent TWMZ results [10-15] however, it was often found that a similar bandwidth was

only achieved with very short devices (~1mm or less) as well as high bias voltages (frequently 3~5V), both of which limit the modulation efficiency. High V_π and associated high drive voltages increase power consumption and make the devices less compatible with advanced CMOS, which is usually constrained by low-breakdown voltages. For long devices [14,15], in addition to smaller bandwidth, they were demonstrated with high insertion loss on the phase shifter making it difficult to fit in a practical system link budget. In summary, further device improvements remain to be made for high-speed low voltage modulators with low loss.

On the topic of data rate versus small-signal bandwidth, we further comment that although an eye-diagram is a direct demonstrator of the device data transmission capability, it is hard to quantify without careful referenced measurements. For example, large driving signals take advantage of the nonlinear portion of the cosine transfer function of an MZ, making it possible to pass high data rate bit stream with otherwise insufficient device bandwidth; the ratio between small-signal device bandwidth and data rate could be 50% or even lower while it is still possible to successfully demonstrate an eye-diagram measurement, as shown in [11]. Thus eye-diagram is not a suitable standalone *device* performance indicator as compared to small-signal bandwidth measurement for depletion-mode devices (considering that the devices operate entirely in the PN junction reversed-biased regime and do not behave significantly nonlinearly). We suggest that small-signal bandwidth measurements should be routinely presented for device papers in this area in the future, for ease of comparison between results.

In this paper, we present a 3mm long, 30GHz bandwidth differential-drive silicon TWMZ modulator based on a lateral PN junction with low reverse bias. The phase shifter $V_\pi L_\pi$ is 2.7V-cm (a small-signal V_π of 9V) and the insertion loss on the phase shifter is only 3.6dB. At similar bandwidth this device shows the lowest V_π and lowest drive voltage requirement due to differential-drive, or at similar V_π it shows the highest bandwidth as well as the lowest insertion loss on the active phase shifter [10-15]. The combined device metrics show significant improvement compared to the state of the art. The main part of the paper is organized as the following. Section 2 describes the fabrication process, identifies key design tradeoffs and presents design details of the device. Section 3 presents the measurement results, compares them to simulation results to validate the design model and provides discussions about several RF effects regarding TWMZ design that were not addressed in previous publications.

2. Device design and fabrication

2.1 Fabrication process

The device presented in this work was fabricated at the Institute of Microelectronics (IME)/A*STAR [17] through an OpSIS Multi-Project Wafer (MPW) run [18]. The fabrication process was very similar to that in [16] with the main difference being that in this work we employed six implant layers instead of four in silicon, and they were: lightly doped P and N for forming the junction in the waveguide core, intermediate density P+ and N+ for reducing series resistance without inducing excessive optical loss, and heavily doped P++ and N++ implant for low resistance silicon far away from the waveguide and for forming low resistance metal-to-silicon contact - no silicidation was used in the fabrication process, the contact was formed directly between aluminum and heavily doped silicon. The traveling-wave phase shifter cross-section is illustrated in Fig. 1 and the microscope photo of the fabricated device is shown in Fig. 3(b). The wafer was an 8" Silicon-on-Insulator (SOI) from SOITEC with 220nm top silicon, 2μm buried oxide layer and 750 Ω-cm high resistive silicon substrate. The silicon slab thickness was 90nm and ridge waveguide width was 500nm. The top metal Aluminum was used for the traveling-wave electrodes, and it was 2μm thick, mostly situated above dielectric materials in the back-end stack. Other metal and dielectric material properties and thicknesses as well as fabrication steps were identical as they were in [16].
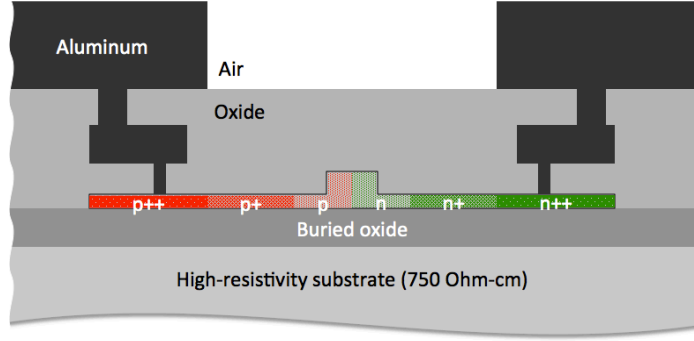
Fig. 1. Simplified device cross-section, not to scale.

2.2 Overall device design considerations

In this section we briefly review the TWMZ design model and present useful design tradeoff relations to facilitate further discussions in this paper. The cross-section of the TWMZ shown in Fig. 1 is considered as a PN junction loaded transmission line and its equivalent circuit model is schematized in Fig. 2. $R_{tl}(f)$ is the frequency-dependent metal skin resistance in Ω/m, and has a $\sqrt{f}$ dependence in principle, C_{tl} and L_{tl} are the capacitance and inductance between the metal traces in the units of F/m and H/m respectively. C_{pn} is the PN junction capacitance (in F/m); the total amount of silicon series resistance from the electrodes to the edges of the junction depletion region is captured in R_{pn} (in Ω-m). We further define the junction intrinsic RC bandwidth as $f_{rc} = \dfrac{1}{2\pi R_{pn} C_{pn}}$ and approximate the device impedance as $Z_{dev} = \sqrt{\dfrac{L_{tl}}{C_{tl} + C_{pn}}}$ which is accurate when the frequency is well below the intrinsic RC bandwidth, i.e. $(f / f_{rc})^2 \ll 1$.
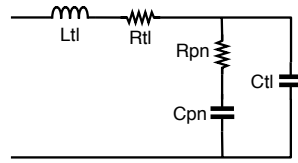

Fig. 2. Schematic of the simplified equivalent circuit of the PN
junction loaded transmission line

The bandwidth of a TWMZ modulator is mostly determined by the RF loss due to R_{pn}, if RF and optical velocities are closely matched. To make this clear we can look at the overall RF field loss coefficient (in the unit of Neper/m), which can be expressed as [19]

$$\alpha = \alpha_{metal} + \alpha_{silicon}$$

$$\approx \frac{1}{2}\frac{R_{tl}(f)}{Z_{dev}} + \frac{2\pi^2 f^2 R_{pn}C_{pn}^2 Z_{dev}}{1+\left(\dfrac{f}{f_{rc}}\right)^2}$$

(1a)

$$= \frac{1}{2}\frac{R_{tl}(f)}{Z_{dev}} + \frac{\pi f^2 C_{pn} Z_{dev}}{f_{rc}\left(1+\left(\dfrac{f}{f_{rc}}\right)^2\right)}$$

(1b)

where α_{metal} and $\alpha_{silicon}$ are the loss due to metal series resistance and lateral silicon resistance respectively. Let us refer to the first term as R_{tl} loss and the second term as R_{pn} loss. At high frequencies, the second term usually dominates because of its f^2 dependence, whereas $R_{tl}(f)$ has a $\sqrt{f}$ dependence. Incidentally, this can be seen clearly in Fig. 4(g), a simulation plot of the actual device under discussion.

For the moment, let us assume perfect velocity match and neglect other non-ideal RF effects (such as reflection, multi-modal behavior and etc.), a straightforward relation between EO 3dB bandwidth $f_{EO,3dB}$ and achievable device length L_{dev} can be derived as [20]:

$$\frac{1-e^{-\alpha(f_{EO,3dB})L_{dev}}}{\alpha(f_{EO,3dB})L_{dev}} = \frac{1}{\sqrt{2}} \Rightarrow \alpha(f_{EO,3dB})L_{dev} \approx 0.74\,Neper = 6.4dB$$

(2)

This is the "6dB" rule-of-thumb frequently referred to in publications about TWMZ, i.e. the RF 6dB (more accurately 6.4dB) bandwidth is close to the EO response 3dB bandwidth.

For the sake of simplicity let us further assume the desired bandwidth $f_{EO,3dB}$ is sufficiently low compared to the intrinsic RC bandwidth of the junction so that $(f_{EO,3dB}/f_{rc})^2 \ll 1$. Usually the TWMZ design is in the "low loss" regime of the transmission line model where this assumption naturally stands. Inserting Eq. 1 into Eq. 2, and we get

$$L_{dev} = \frac{0.74}{\dfrac{1}{2}\dfrac{R_{metal}(f_{EO,3dB})}{Z_{dev}} + 2\pi^2 f_{EO,3dB}^2 R_{pn}C_{pn}^2 Z_{dev}}$$

$$\approx \frac{0.74}{2\pi^2 f_{EO,3dB}^2 Z_{dev}}\frac{1}{R_{pn}C_{pn}^2}$$

(3a)

$$= \frac{0.74}{\pi f_{EO,3dB}^2 Z_{dev}}\frac{f_{rc}}{C_{pn}}$$

(3b)

The approximation before arriving at Eq. 3a is based on that R_{pn} loss is much larger than R_{tl} loss at frequencies near $f_{EO,3dB}$.

A few scaling trends can be derived from Eq. 3a and 3b, which quantify the tradeoffs in the seemingly complicated design space:

(I) It becomes apparent that getting low V_π at high frequency is increasingly difficult, since $L_{dev} \propto \dfrac{1}{f_{EO,3dB}^2}$, consequently $V_\pi \approx (V_\pi L_\pi)/L_{dev} \propto f_{EO,3dB}^2$.

(II) In general, to design for certain impedance and bandwidth the achievable device length L_{dev} and V_π have the following scaling trends with respect to PN junction parameters:

$$L_{dev} \propto \frac{1}{R_{pn}C_{pn}^2}, V_\pi \propto (V_\pi L_\pi)R_{pn}C_{pn}^2$$

(4)

Obviously, a reduction in R_{pn} is directly reflected in a reduction in V_π (for certain bandwidth design target). Highlighted in Eq. 4 is another key point. In an attempt to improve junction modulation efficiency (reducing $V_\pi L_\pi$) the factor $(V_\pi L_\pi)R_{pn}C_{pn}^2$ should be evaluated. A reduction in $V_\pi L_\pi$ is likely to come at the cost of increased C_{pn}. An increase in $(V_\pi L_\pi)R_{pn}C_{pn}^2$ implies that the reduction in $V_\pi L_\pi$ does not ultimately lead to the reduction of the device V_π. Therefore, a low doped, low capacitance density junction could be a more advantageous for traveling-wave design, which is the case of the design reported in this paper.

(III) Designing at lower device impedance Z_{dev} is advantageous, because $L_{dev} \propto \dfrac{1}{Z_{dev}}, V_\pi \propto Z_{dev}$,

holding junction parameters constant. Note that the impedance Z_{dev} is not the termination impedance but the RF impedance of device itself. The effect of termination impedance on device performance will be addressed in Section 3.2. Assuming the device is in fact terminated with Z_{dev}, we can then conveniently evaluate the drawback of using low impedance design, which is mainly some loss of the incoming drive voltage, if the driver is at impedance Z_0 that is higher than Z_{dev}. The ratio of voltage dropped on the

device (V_{dev}) versus the driver output voltage (V_0) is $\dfrac{V_{dev}}{V_0} = \dfrac{2Z_{dev}}{Z_{dev}+Z_0}$. For example, this voltage-intake

factor is 67% for a 25Ω device terminated with 25Ω driven by a 50Ω driver. However, the achievable device length at 25Ω is approximately twice as it would be for a 50Ω design based on Eq. 3, therefore overall the 25Ω design would be more advantageous. The device length doubling is of course a rough estimate, due to the omission of metal loss, which could be significant if target impedance is extremely low.

It is also worth noting that single-drive push-pull modulators [21] demonstrated an elegant way to ease the design of 50Ω device impedance while conveniently maintaining matched RF and optical velocities. Due to halving the junction capacitive loading to the transmission line electrode, the bandwidth-limiting R_{pn} loss is approximately halved (according to Eq. 1(b), keeping f_{rc} constant) and therefore very long devices are possible at high speeds. However, doubled device length combined with single-drive operation yields approximately the same drive voltage requirement as it is for a conventional differential-drive TWMZ device, while doubling the device length implies high optical insertion loss, which is a drawback that needs to be weighed against the benefits associated with such single-drive designs.

2.3 PN junction design

The waveguide PN junction phase shifter is the core component of an MZ modulator; its metrics largely determine the achievable overall device performance, as shown in Eq. 3 and Eq. 4. In addition to providing a low $(V_\pi L_\pi)R_{pn}C_{pn}^2$ factor, the PN junction design also needs to achieve low optical insertion loss.

We chose lightly doped P and N to form the junction in the waveguide with the P side average doping concentration being around 5e17/cm^3 and N side being close to 3e17/cm^3. The junction line was designed to be at the center of the waveguide, with no intentionally added intrinsic region width. This low-doped PN junction is in favor of the efficiency versus loss tradeoff, characterized by the figure-of-merit F_{dB-V} (in dB*V) as defined in [22,23]. Also, it helped achieve a low $(V_\pi L_\pi)R_{pn}C_{pn}^2$ by maintaining a low C_{pn} and competitive $V_\pi L_\pi$.

To achieve a low R_{pn} with low loss, we employed a 3-level side-doping configuration as illustrated in Fig. 1, with carefully chosen doping density and doping profile. We selected P+ and N+ doping density of 2e18/cm^3 and 3e18/cm^3 respectively and optimized the doping profile. The onset of doping to the edge of the waveguide is defined as "clearance". The clearance of P+ and N+ doping were 120nm and 140nm respectively. The P++ and N++ doping were on the level of 1e20/ cm^3 and their clearance were both

950nm and the doped region extended laterally until they reached the electrode contact regions that were 3.95μm away from the edge of the waveguide. A breakdown of optical loss and resistance of the various regions is presented in Table 1 below.

Table 1. Optical loss and resistance breakdown

	N & P doped waveguide core		N & P doped slab region		N+ doped slab region		P+ doped slab region		N++ & P++ doped region		Total	
	R	IL	R	IL	R	IL	R	IL	R	IL	R	IL
Simulation	1.5	6.8	1.6		1.1	0.97	2.5	0.53	0.49	0.01	7.2	8.3

Notes: "R" denotes resistance in Ω-mm, "IL" denotes insertion loss in dB/cm. The IL reported for waveguide core includes the loss of N and P doped slab region due to simulation setting. IL numbers only include free carrier absorption loss at 0V bias, and do not include intrinsic waveguide loss.

Based on implantation process modeling and device simulation [24], C_{pn} was 280 pF/m at 0V and 220 pF/m at -1V bias, thus f_{rc} at -1V bias reached 100 GHz. The simulated $V_\pi L_\pi$ was 1.7 V-cm at -1V bias.

2.4 Traveling-wave electrode design

In light of the observation (III) in the end of Section 2.1, we continued to use a 33~37Ω impedance design similar to [16] instead of designing at 50 Ω. This is also a convenient impedance to design with our junction capacitance C_{pn} while achieving velocity matching condition and low RF loss. Another consideration was that if the device were properly terminated with matching impedance, this device would still provide an acceptable S11 (<-10dB), when tested in 50Ω environment or integrated with 50Ω drivers.

However, we do not deem it a fundamental requirement to comply with 50Ω standard RF interfaces, because eventually and especially for on-chip applications the TWMZ devices are likely be closely integrated with custom drivers, in which cases the short length (or even zero length) electrical connection as well as the availability of custom designed low impedance drivers would make it possible to freely choose any impedance as long as it advances the overall device and system performance. For example, numerous laser drivers have been designed at very low impedances [25] for efficient driving.
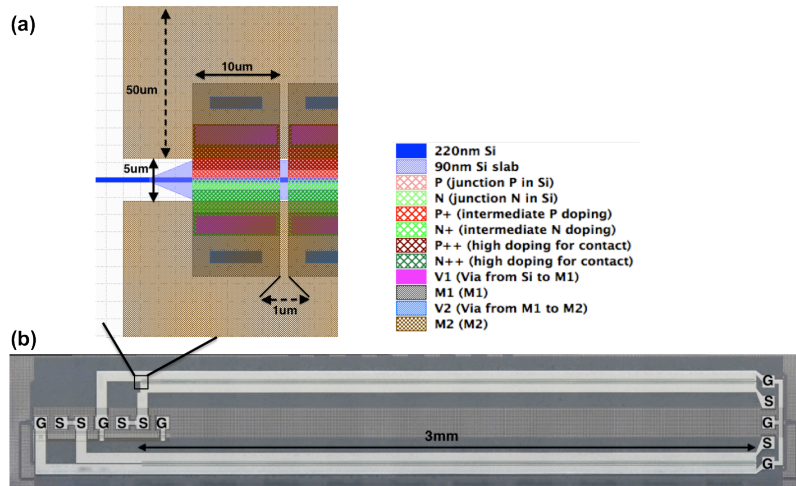
Fig. 3. (a) RF layout dimensions (b) Device microscope photograph

The device layout and microscopic photograph is shown in Fig. 3. We used a Ground-Signal (GS) coplanar transmission line electrode to drive each arm. The GS lines have 50μm trace width and 5μm gap. The length of the phase shifter is 3mm. The separation between the two arms is 400μm center-to-center. The traces used the 2μm thick aluminum layer (M2) in the process. The layout of the via-stack from M2 down to silicon was mainly determined by design rules and considerations to achieve sufficiently low resistances for vias and metal-to-silicon contacts. The detailed PN junction and side doping configurations were described in Section 2.3. It is worth noting that the phase shifter in the actual TWMZ only has ~90% of its length loaded with PN junction, due to striation as illustrated in Fig. 3(b). The striation in doping was to ensure the current flows in the metal traces toward the wave propagation direction, as opposed to flowing in the silicon.

At the driving end (the right side in Fig. 3(b)), a GSGSG pad set was used to deliver differential driving signal to the device. A transition was made on chip from GSG to GS. At the termination end (the left side in Fig. 3(b)), a GSSGSSG pad set was used, offering four 50Ω ports. Each device arm was associated with two 50Ω ports in parallel, allowing 25Ω termination through a GSSGSSG RF probe and off-chip resistors. Other values of termination impedance would be less convenient, but is possible to implement by bonding the photonics chip to a high-speed printed circuit board (PCB) via short-length bond wires, and using surface-mount low parasitic resistors on the PCB. On the other hand, the GSSGSSG pad set allowed us to take the RF S-parameter as discussed in detail in Section 3.2.

Simulated RF characteristics of the transmission line electrodes with and without PN junction loading is presented in Fig. 4 (a)-(f). First, the metal traces were simulated in HFSS [26], and then loaded line characteristics were calculated based on the circuit model in Fig. 1(b). The presented curves that involve PN junction, i.e. the dotted traces in Fig. 4 (e) and (f) and the entire plot of Fig. 4(g), were calculated at 0V bias condition and with the 90% junction loading factor taken into account. Near 30GHz, R_{tl} is 8.1 kΩ/m, L_{tl} is 420 nH/m, and C_{tl} is 120 nF/m. Loaded with PN junction, the impedance is 34 Ω and RF index is 3.78 at 30GHz. The RF loss is presented in Fig. 4(g) with the total loss, and loss due to R_{tl} and R_{pn} plotted separately and it is clear that R_{pn} loss is the dominating source of RF loss at high frequencies. In this plot Case 1 trace was obtained with simulated R_{pn} and C_{pn}, i.e. 7.2 Ω-mm, and 280pF/m, whereas Case 2 was using 15 Ω-mm and 230pF/m to approximate the measured device. The increase in R_{pn} in fabricated device is mainly attributed to the higher sheet resistance in the light P and N doping as well as higher contact resistance from metal to P++ doped silicon, which will be discussed in Section 3.
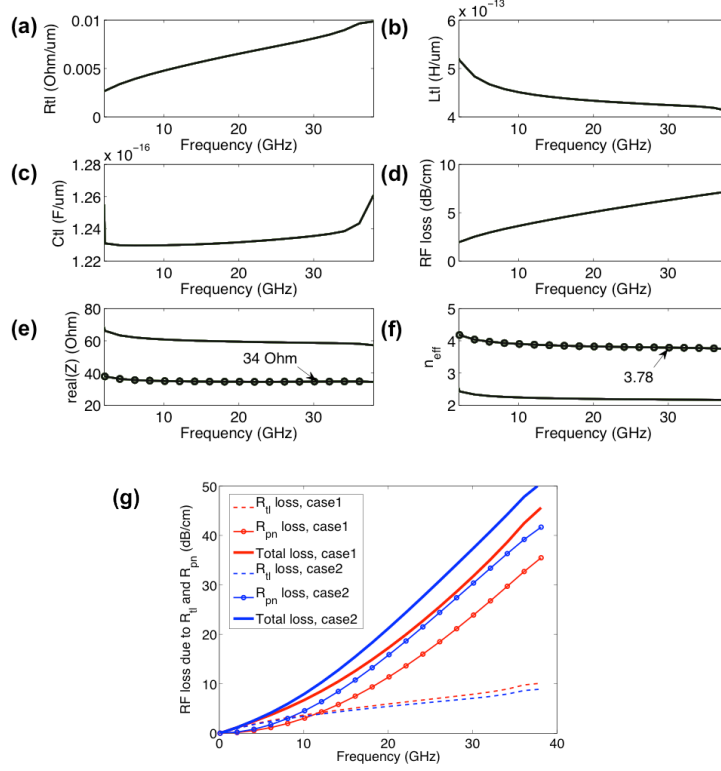
Fig. 4. (a-f) Simulated unloaded TL (solid line) and junction-loaded TL with 0V bias (solid line with dots), the frequency axis range is set to 2GHz ~ 38GHz to eliminate artificial simulation data processing errors (g) Simulated RF loss of the device under investigation, Case1 is based on simulated C_{pn} and R_{pn} and Case2 is based on measurement-corrected C_{pn} and R_{pn}

3. Measurement results and discussions

3.1 DC $V_\pi L_\pi$ and insertion loss

We first measured the optical transmission and DC performance of the device. The optical test setup used an Agilent 81980A tunable laser and an 81636B detector to record the device transmission spectra. The intentional imbalance of the device was 100μm and the free spectral range was about 5.7nm. We tracked the null in the spectrum to generate phase shift versus applied voltage on one arm, from which $V_\pi L_\pi$ was calculated. The results are shown in Fig. 5. Incidentally, there are some ambiguity and discrepancy about the definition of $V_\pi L_\pi$ in the literature. One way to report $V_\pi L_\pi$ is based on an actual π phase shift [27,28]. This test protocol require devices of various lengths to get a $V_\pi L_\pi$ versus V_π (or L_π) curve and could be difficult for short devices (high voltages). Here we adopted an alternative approach: the $V_\pi L_\pi$ versus applied voltage relation is generated by the measurement of the phase shift $\Delta\phi_{dut}$ versus applied voltage $V_{applied}$ on one phase shifter of certain length L_{dut}, and simply $V_\pi L_\pi = \dfrac{\pi}{\Delta\phi_{dut}} V_{applied} L_{dut}$. The curve $V_\pi L_\pi$ versus $V_{applied}$ is basically $V_\pi L_\pi$ versus V_π. This approach was widely used in publications on silicon modulators, including several in the references list, for example [11], [13,14], [23] and [24].
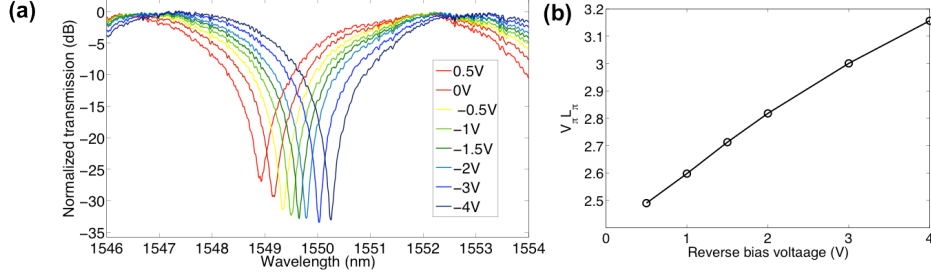
Fig. 5. (a) Optical spectra versus applied voltage (b) $V_\pi L_\pi$ versus applied voltage

At -1V bias the measured phase shifter $V_\pi L_\pi$ was 2.7V-cm. Further measurements over 5 different chips showed a good uniformity. Taking into account the 90% loading factor, the $V_\pi L_\pi$ of a fully doped waveguide phase shifter would be 2.43V-cm, higher than the simulated 1.7V-cm. The measured C_{pn} was 230pF/m at 0V and 190pF/m at -1V bias for a fully doped waveguide phase shifter, lower than the simulated value 280pF/m at 0V and 220pF/m at -1V. We further measured silicon resistors with various doping types, doping concentrations and silicon thicknesses, and revealed that P++ or N++ doped silicon resistance agreed with simulation within 5%. However, P+ or N+ doped silicon showed ~30% higher resistance than simulation, and P or N doped resistance showed ~50% higher resistance than simulation. Combining the higher $V_\pi L_\pi$, lower C_{pn} and higher resistance of P or N doped silicon resistance, we suspect the discrepancies could be due to: physically applied implantation dose being smaller than simulated, and possible incomplete ionization of the dopant. Other fabrication inaccuracies are harder to be verified or excluded.

The on and off chip coupling were through grating couplers. The device insertion loss was obtained by comparing the maximum transmission of the MZ spectrum to a grating coupler loop to de-embed the coupler insertion loss. Then the routing waveguide loss was subtracted, and we arrive at the device insertion loss of 6.2dB that consist of two simple Y-junctions and the phase shifter. We note that the Y-junction in this particular device was not carefully designed and has a high insertion loss of 1.3dB each. Therefore the loss due to the phase shifter was only 3.6dB (averaged from multiple chips with a standard deviation of 0.37dB). The reduction of the loss in Y-junction would be straightforward, because recently a 0.3dB insertion loss optimized Y-junction with uniform yield was demonstrated and was fabricated in the same batch of wafers [29].

The 3.6dB±0.37dB phase shifter insertion loss can be broken down as follows. The waveguide intrinsic loss was measured to be 1.98±0.29dB/cm from 5 samples on the same wafer, i.e. a ~0.6dB contribution to the phase shifter loss. Therefore the various dopants (junction and side doping) introduced 3.0dB±0.38dB loss. Considering the 90% loading coefficient, we can back calculate the free carrier absorption loss was 11.1±1.5dB/cm, whereas the simulated value is 8.3dB/cm. The discrepancy could be excess loss due to P+ and N+ misalignment error (the 3σ of the overlay accuracy was a large fraction of the doping clearance) or a slight change in waveguide dimensions inducing change in optical mode overlap with P+ and N+ dopants. Incidentally, we measured PN junction doped waveguides that are without the side doping P+, N+, P++ and N++. The measured free carrier loss was 6.3dB/cm on average, which was very close to the simulated 6.8dB/cm. This made it more likely the extra loss seen in the TWMZ phase shifters was due to P+, N+ doping and etc.

3.2 Small-signal bandwidth measurement

The EO frequency response of the TWMZ was characterized using an Agilent 67GHz Vector Network Analyzer (VNA), and an U2T XPDV3120R-VF-VP 70GHz bandwidth photodetector. The EO S21 is presented in Fig. 5. This measurement was done through on-wafer probing with a 40GHz rated Cascade ACP GSGSG driving probe and a 20GHz rated Cascade Unity GSSGSSG probe with off-chip resistors for 25Ω termination. The VNA drove only one device arm at a time; the unused arm was properly

terminated at both the driving and termination end with 50Ω and 25Ω respectively. This "full-termination" scheme closely resembles the actual operating condition of a differential drive modulator. The probes were not de-embedded from the frequency response and the RF S21 roll-off of the GSGSG probe was 0.5dB near the device bandwidth. Reverse bias was applied through the bias-tee in the VNA.
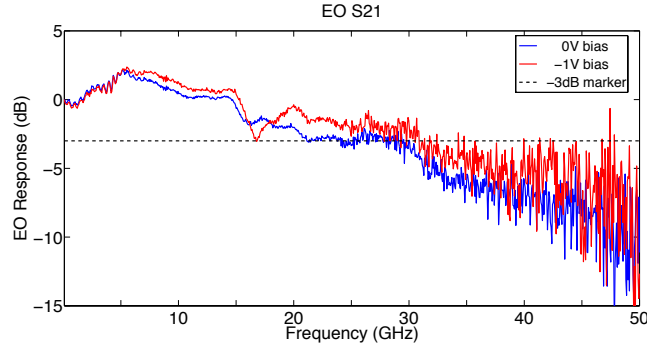

Fig. 5 EO S21 at 0V and -1V bias

30GHz bandwidth was achieved for both arms at 1V reverse bias. The same bandwidth was almost reached with 0V bias (a long plateau in the EO S21 coincided with the -3dB line between 23GHz and 30GHz). We observed two distinctive features of the EO S21: the peaking near 5GHz and the notch near 17GHz. These two features were consistently observed across many devices on both arms. We will explain them based on RF measurements.

The RF S-parameter measurements were done with the 40GHz GSGSG probe at the driving side with one GSG port connected to VNA Port 1 and the other GSG port attached to 50Ω to terminate the unused arm. At the termination end, a 40GHz GSSG probe was used with one GS port connected to VNA Port 2 and one GS port attached to 50Ω. It presents 25Ω to the modulator arm under test and receives RF through signal. We had to left the termination end of the untested arm open due to the lack of a high speed GSSGSSG probe. The RF calibration included the cabling but could not include the probes, due to the lack of a GSG-to-GS calibration substrate. The uncalibrated probes were responsible for the fine-pitch ripples on the S-parameters traces, most visible on S11 due to their low magnitude. The measurement results are shown in Fig. 6(a).
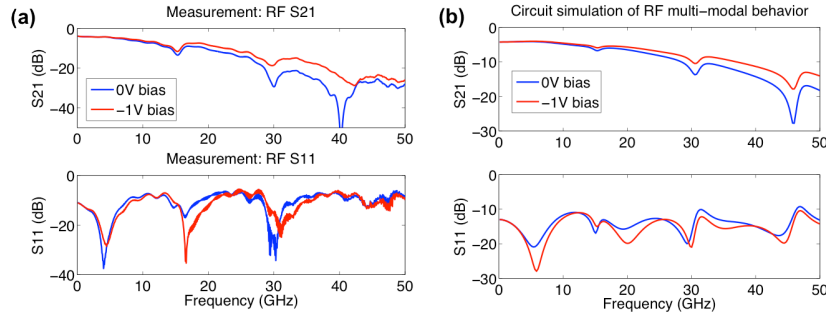

Fig. 6. (a) RF S-parameters measurement (b) circuit simulation to verify hypothesis of RF multi-modal behavior

First of all, we can use RF S11 and S21 to back calculate the RF index and RF loss. The RF index can be obtained by $n_{rf} = \dfrac{c}{2L_{eff}\Delta f}$, where c is the speed of light in vacuum, L_{eff} is the effective RF length taking

into account of the input and termination (estimated to be 3.3mm based on simulation), and Δf the spacing of S11 null locations (measured to be 12GHz). Therefore RF index was calculated to be 3.8, and is close to the optical group index 3.9.

　　To calculate RF loss and RF 6.4dB bandwidth, we should note that the measured RF S21 starts at -3.9dB rather than close to 0dB. This was due to the 50Ω-driving, 25Ω-termination testing configuration, which results in a 67% voltage-intake at low frequencies (see Section 2.1). In principle it should be -3.5dB, the slightly lower value in measurement was likely due to the series resistance on the long metal traces and probe contact resistance. The RF S21 6.4dB bandwidth was 20GHz and 23GHz for 0V and -1V bias, respectively. As mentioned earlier we observed higher resistance in various dopants doped silicon. In addition, we measured the contact resistance between metal and P++ doped silicon to be significantly higher than anticipated and equivalently contributes to 5Ω-mm to R_{pn} . We therefore calculated that in the fabricated device R_{pn} is 15Ω-mm instead of the simulated 7.2 Ω-mm. This measurement-corrected resistance in combination with the measured C_{pn} allowed us to re-simulate the RF loss based on measurements, as shown in Fig. 4(g) (Case2). It suggests a RF 6.4dB bandwidth of 20GHz at 0V, in excellent agreement with measurement.

　　The difference between RF 6.4dB bandwidth and EO S21 3dB bandwidth is due to the mismatch between device impedance and termination impedance. This assessment can be evaluated analytically by expressing the RF voltage amplitude on the transmission line as forward and reverse propagating waves due to reflection then an overlap integral with the forward propagating optical wave would generate the EO response [20]. For the 33Ω impedance device we simulated three different termination scenarios and they are shown in Fig. 7. In these simulations, we chose an approximate f^2 dependent RF loss function to have RF 6.4dB bandwidth of 23GHz to emulate measured performance at -1V bias. In the case where the termination was exactly matched to device impedance (i.e. $Z_{term} = 33\Omega$), as expected the EO 3dB bandwidth was almost exactly at the RF 6.4dB bandwidth. For high impedance termination case (i.e. $Z_{term} = 50\Omega$), the device bandwidth was very limited and the last crossing of the -3dB line was only at 13GHz, this is caused by the reflected wave with an undesired phase shift. On the other hand, for the low impedance termination case (i.e. $Z_{term} = 25\Omega$), which is close to the measurement condition, the reflected wave enhanced the EO response. Near 5GHz we observed peaking of similar magnitude as that in the measurement, the peaking effect is most pronounced at low frequency S11 nulls primarily due to less phase mismatch (and secondarily due to less RF loss). The device showed close to 29GHz bandwidth. This is a close match to measurement results, validating our theory. This indicates an advantage of using termination impedance that is lower than the device impedance. As we discussed earlier, at low frequencies the voltage on the device can be evaluated by $\frac{V_{term}}{V_0} = \frac{2Z_{term}}{Z_0 + Z_{term}}$ and a voltage-intake factor of 67% is obtained for 25Ω termination versus 50Ω termination. Considering a bandwidth extension ratio of 2.2 (29GHz / versus 13GHz), the 25Ω termination case appeared to be more advantageous overall.
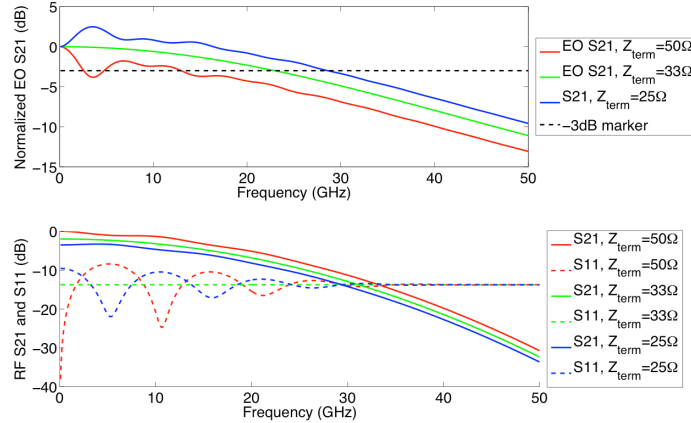
Fig. 7. Analytical modeling of EO response with respect to termination impedance

Finally, we address the other distinctive signature in the EO S21: the notches in the spectrum. Due to its low magnitude, the notch in the EO S21 would not noticeably degrade eye-diagrams, as was suggested by our eye-diagram simulation comparisons between artificially smoothened EO S21 and measured EO S21. However, the notches are certainly detrimental features and could lead to serious problems in certain designs if we do not develop a good understanding of its root cause.

Observing the RF S21, it is evident the notches and steps in EO S21 occur at similar locations as the notches in RF S21. The most visible ones on EO S21 are near 17GHz and 30GHz. The magnitude of the RF S21 notch at 17GHz was 3~4dB, which could mostly explain the corresponding notch in the EO S21. To explain the notches in RF S21, we propose a hypothesis that the GS-SG structure is multi-modal. In more detail, when we were testing one device arm, i.e. driving one GS transmission line, we were effectively driving a GS-G structure. The G trace far away has a non-negligible RF interaction with the S trace. This GS-G structure supports two modes due to asymmetry (structure, dielectrics distribution and PN junction loading). A full structure HFSS simulation was challenging due to the large computation domain (long device length and large lateral span), but an analytical analysis could be formulated based on [30]. As a simplification for weakly coupled lines we assume the GS-G supports the 33~37 Ω mode ("main" mode) we originally designed between the S and the nearby G trace, and the GS-G also supports a stray mode that is mostly between the S and the far away G trace. We model the two modes as two independently propagating modes only connected at the beginning and end of the line. The combined line was driven by a 50Ω source and terminated by 25Ω. We used the TWMZ parameters described earlier for the main mode, and estimated the capacitance between the S trace and the far away G trace is C_{stray}=~20pF/m, using two-wire transmission line equations [19]. To avoid complicated circuit models, we picked reasonable constant metal skin resistance as opposed to a frequency-dependent multi-resistor-inductor network (which is responsible for the large simulation errors in S21 notch amplitude and S11 amplitude and null location). But, our simple model appeared to be sufficient as a qualitative validation. Using a circuit simulator [31], we obtained the traces in Fig 6(b) with stray inductance between S and side G as L_{stray}=4.2mH/m. Qualitatively, Fig. 6(b) agrees well with Fig. 6(a), and validates our multi-modal hypothesis.

In light of this observation we further comment that, notches in RF S21 were observed in previous demonstrations of TWMZ modulators that were based on a GSG layout (or a GSGSG layout by combing two GSG arms), where the PN junction was loaded only in one of the two GS slots. Examples include Fig. 5 in [11], Fig. 9 in [12], Fig. 4 in [14] and likely Fig. 4 in [13]. Many demonstrations did not present EO or RF S21, therefore it is difficult to have a more complete summary. But, according to our simulations in HFSS of a few relatively compact GSG modulator structures, notches were usually present in RF S21. It is very likely that the notches in these demonstrations are due to multi-modal RF behavior

as well: the one-side junction loading makes the GSG structure highly asymmetric in a similar fashion as the GS-G structure we discussed above and this RF multi-modal property is expected to exhibit detrimental effect given that the device is sufficiently long and/or the testing frequency is sufficiently high.

A simple remedy to both the GSG structure and GS-G structure is that one needs to periodically tie together the ground planes that are on both sides of the S trace, so that effectively there is only one large ground plane interacting with the S trace, ensuring only one RF mode is supported between S and G. The spacial period of the "G-tie" should be much smaller than the beat length of the lowest two eigenmodes of the originally multi-mode structure.

3.3 Eye-diagrams

We further demonstrated high-speed eye-diagrams with differential drive. The available sample for the eye-diagram measurements exhibited similar V_π and EO S21 bandwidth as reported in previous sections. The measurement was set up as following. A pair of differential 40Gb/s 2^{15}-1 pseudorandom binary sequence (PRBS) was generated by a Centellax TG1P4A PRBS source, amplified by a pair of Centellax OA4MVM3 driver amplifiers, and then attenuated by passive attenuators (rated for DC-23GHz) to the desired amplitude before being applied to the device under test through a Cascade 40GHz rated GSGSG probe. DC bias voltages were applied to each modulator arm through bias tees inserted before the attenuators. The device probing and termination configuration were the same as the S-parameter measurements, with slightly different cabling. The optical output of the device was passed through an Erbium Doped Fiber Amplifier (EDFA), an optical bandpass filter with 3.5nm bandwidth and then sent to the optical module (Agilent 86109B) of an Agilent 86100B digital communication analyzer (DCA).
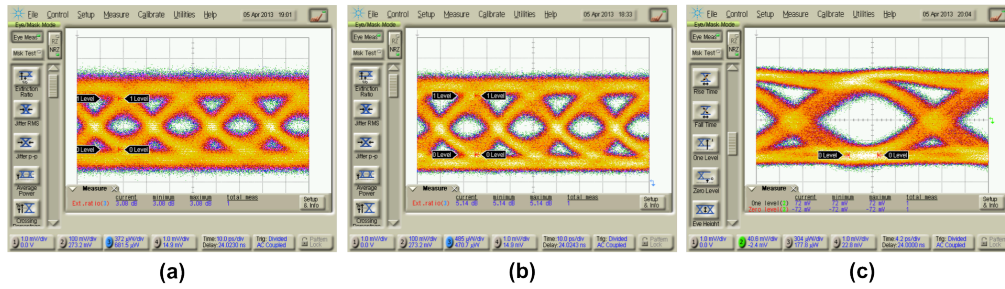

Fig. 8. (a) and (b): optical eye-diagrams at 40Gb/s with differential-drive: (a) 0V bias and 1.6V_{pp} drive voltage, 3.1dB extinction ratio was achieved with bias loss of 1.4dB. (b) 0.25V reverse bias and 2.5V_{pp} drive voltage, 5.1dB extinction ratio was achieved with bias loss of 1.7dB. (c) a typical electrical eye-diagram of the driving signals

We report on eye-diagrams with different drive voltages and modulator bias losses in Fig. 8(a) and Fig. 8(b). The bias loss is the excess loss due to modulator biasing, to quantify how much the bit "1" optical output is below the maximum transmission. For example, 3dB bias loss means bit "1" is at the quadrature point. The differential drive voltage signals before connected to the GSGSG probe were verified by electrical eye-diagram measurements, based on which we can accurately report the drive voltages in a 50Ω test environment. A typical 40Gb/s electrical eye-diagram of the driving signal is shown in Fig. 8(c). The actual drive voltage received by the device is slightly lower than the reported drive voltage due to the voltage-intake factor that we discussed before. We observed a slight output asymmetry of the electrical amplifiers and attenuators on the two data paths, but the difference was within 5%, and we report the averaged drive voltage values below.

Using a 1.6V_{pp} drive voltage and 0V DC bias, 3.1dB extinction was achieved with a very low 1.4dB bias loss, as shown in Fig. 8(a). The power consumption can be calculated as following. At an impedance of 50 Ω, an ideal 1.6V_{pp} NRZ signal centered at 0 V carries 12.8 mW of power. At 40Gb/s, the energy per bit is 640fJ/bit. Due to the availability of test equipment only 40Gb/s operation was demonstrated,

although we expect the device to be capable of passing higher data rate bit streams based on simulations, which would result in further reduction of energy per bit.

The achievable extinction ratio (ER) in the eye-diagrams can be traded off with drive voltage and bias loss. For example, with a 2.5V_{pp} drive voltage and a 0.25V revere bias, 5.1dB extinction was obtained with 1.7dB bias loss, as shown in Fig. 8(b). The observed ER is lower than anticipated based on the phase shifter static performance (phase shift and dynamic loss versus applied voltage). The reduced extinction and reduced eye vertical opening is partly due to the limited bandwidth in the testing system in addition to the device itself. The electrical eye-diagrams mentioned above measured the drive signal immediately before the RF probe connected to the device, that is it included the PRBS source, amplifiers, bias tees, attenuators and cables. From the electrical eye-diagram in Fig. 8(c), we measured a 10% to 90% rise time of roughly 15ps, which amounts to approximately 23GHz bandwidth and leaves a tight margin for the device. In addition to the limited system bandwidth, optical noise due to the EDFA further degraded the eye opening.

Conclusions

To summarize, in this paper we address the design and characterization of a high performance silicon PN junction traveling-wave Mach-Zehnder modulator. The key underlying design tradeoffs are identified and incorporated into the device design. A device is then presented with significant performance improvement compared to the state of the art.

A PN junction design should maintain a low $(V_{\pi}L_{\pi})R_{pn}C_{pn}^2$ factor to enable low V_{π} with high device bandwidth. Modulation efficiency needs to trade effectively with optical loss, indicated by the F_{dB-V} figure-of-merit. For both considerations we chose lightly doped PN junction with optimized 3-level side doping.

We have shown that lower device impedance is advantageous for overall device performance, and a 33~37Ω device impedance was chosen for the TWMZ design. Having termination impedance lower than the device impedance has benefit in terms of bandwidth extension while only incurring modest voltage loss. A bandwidth extension factor of 2.2 was achieved while the voltage-intake factor was maintained at a reasonable 67%. Multi-modal RF behavior is proposed and qualitatively verified to be the possible cause for the S21 notches observed in our device as well as several recent GSG modulator demonstrations. A remedy is suggested to combat this. Therefore, performance enhancement and impairment are both possible with respect to the RF design aspect of a TWMZ device, and 6.4dB RF bandwidth is not always a good indicator of 3dB EO response bandwidth..

A 3mm long 30GHz bandwidth differential-drive TWMZ modulator is demonstrated with 1V reverse bias. The device exhibits a small-signal V_{π} of 9V and has a low 3.6dB insertion loss on the phase shifters. 40Gb/s eye-diagrams were demonstrated, and 640fJ/bit energy per bit was achieved with 1.6V_{pp} drive voltage and no DC bias; higher data rates were expected to be possible although not demonstrated due to the limitation of test equipment. Compared to the state of the art, at similar bandwidth this device shows the lowest V_{π} and lowest drive voltage requirement due to differential-drive, or at similar V_{π} it shows the highest bandwidth as well as the lowest insertion loss on the active phase shifter. The combined device metrics show significant improvement compared to the state of the art. Taking into account of the fabrication imperfections, the device behavior was accurately described by device models.

Bandwidth Enhancement of Waveguide-Coupled Photodetectors with Inductive Gain Peaking

Silicon has recently attracted a great deal of interest as an economical platform for integrated photonics systems. Integrated photodetectors are a key component of such

systems, and CMOS-compatible processes involving epitaxially grown germanium for photodetection have been demonstrated. Detector parasitic capacitance is a key limitation, which will likely worsen if techniques such as bump bonding are employed. Here we propose leveraging the complexity available in silicon photonics processes to compensate for this using a technique known as gain peaking. We predict that by simply including an inductor and capacitor in the photodetector circuit with the properly chosen values, detector bandwidths can be as much as doubled, with no undesired effects.

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1. Introduction

Silicon shows promise as an economical platform for integrated photonics systems, due to the large infrastructure in place from the silicon electronics industry, as well as silicon's intrinsic manufacturability [1-3]. However, in many situations, the device performance of silicon is still inferior to that of conventional optical systems, such as III-V semiconductor materials [4, 5] or lithium niobate [6]. One way of circumventing this limitation is to leverage the complexity that is

increasingly available in silicon photonics processes [2, 3]. We will show that with the metal layers typically available in a CMOS-compatible process [7], it is possible to dramatically enhance the performance of waveguide-coupled photodetectors.

Germanium photodetectors are now widely used [8-14] for integrated photodetection on the silicon platform. Typically PIN diodes are used, though photoconductive detectors have also been demonstrated [11, 12]. Germanium can be readily integrated into a silicon system through epitaxy [14]. A significant drawback of using germanium for photodetection at 1550 nm is the relatively low absorption coefficient of 0.2 dB/μm [15], which has prompted some work to be done at 1310 nm where the absorption is much higher [16]. Due to the low absorption, the physical size of germanium detectors often needs to be large in order to achieve high responsivity, which in turn creates a large capacitance. Detectors with areas of 60 μm^2, 370 μm^2 and 700 μm^2 are typical in the literature, with corresponding detector capacitances of 32 fF, 66.7 fF and 200 fF, respectively [9, 10, 8]. Often, the bandwidth of a photodetection circuit can be modeled as a simple RC load. Taking f_c to be the 3-dB frequency (at which point the photocurrent has decreased by a factor of $\sqrt{2}$), C_{pd} the detector capacitance, R_l the load resistance, and R_{pd} the photodetector resistance, which is in general a combination of contact resistance to the n and p regions of a photodiode and the series resistance between the contacts and the photocurrent-generating intrinsic region:

$$f_c = \frac{1}{2\pi C_{pd}\left(R_L + R_{pd}\right)} \qquad (1)$$

The associated circuit is shown in Fig. 1. We note that R_l could indicate the input to a transimpedance amplifier (TIA), or simply a 50-Ω transmission line.
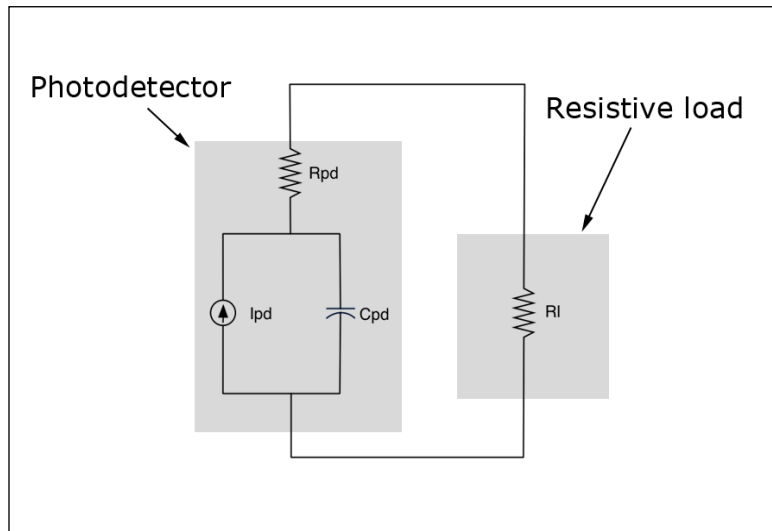

Fig. 1. Equivalent small-signal AC circuit for a photodetector and a simple resistive load. The parasitic capacitance and resistance of the detector is shown. The detector appears as a current source.

Clearly larger detector capacitances will degrade device bandwidth. As a result, a natural avenue for bandwidth improvement has been to decrease device capacitance [17]. A secondary consideration in photodetector design is the transit-time limitation [18]. In a p-i-n detector, free carriers are created in the germanium intrinsic region due to photo-absorption, and they must be swept to the p- or n-doped collection regions. This transit time limits photodetector bandwidth in some situations. A natural approach to decreasing transit time is to narrow the intrinsic region; however, this comes at the expense of increased detector capacitance [18]. Decreasing the relative importance of detector parasitic capacitance will thus be of significance for this aspect of photodetector design as well. For simplicity, we will assume that the photodetectors we describe here are not transit-time limited.

Recently, significant improvements have been made in detector capacitance through using very small area photodetectors, with capacitance values of 1.2 fF demonstrated while still maintaining a responsivity of 0.8 A/W and bandwidths of 45 GHz [19]. Actually, even in this situation, capacitance can become a limitation. It is often desirable to use a load with higher resistance. As we will show, the associated bandwidth for a given RC circuit can still be improved, even for loads of 1 kΩ or more.

There are still several reasons to expect that larger area photodetectors will continue to be used, and that capacitance will remain a limitation. First, these smaller geometries may not be compatible with already existing and well-characterized photonics processes [9, 14, 20]. Second, increasing photodetector power handling levels may require larger area detectors, or equivalently, multiple photodetectors in parallel. It is also sometimes necessary to accommodate more than one mode in a single photodetector in order to support polarization diversity [20]. Finally, if bump bonding is employed to bond an electronic chip, then this too raises the effective parasitic capacitance of the detector [21].

As silicon photonics processing has matured, an increasing level of complexity has become available. It is not uncommon for there to be several layers of metal available in wafer-scale processes [7], as shown in Fig 2., and for silicon-on-insulator (SOI) with a high-resistivity handle wafer to be used [22], allowing high Q inductors. Metal-insulator-metal (MIM) capacitors will also likely be available as CMOS-compatible processes are adapted to address silicon photonics [22, 23]. Crucially, as part of a monolithically integrated back-end, these components can be built directly adjacent to integrated waveguide-coupled photodetectors.
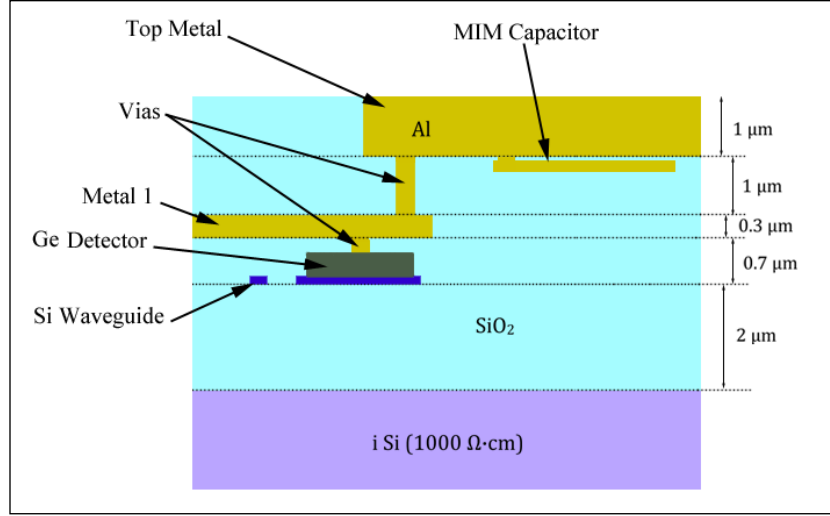
Fig. 2. Typical silicon photonics cross-section formed by combining typical silicon waveguide geometries with two layers from a typical CMOS metal stack. Dimensions are hypothetical and do not refer to a realized process. The active layer of silicon is shown, as well two metal layers, typically formed of aluminum, and a metal-insulator-metal (MIM) capacitor layer. Typically a high-resistivity handle wafer on the order of 1000 Ω-cm or higher is used for RF performance.

Assuming that a thicker, low-resistance metal is available, it should be possible to fabricate high quality inductors if a high-resistivity handle wafer is used [22]. The availability of this component in close proximity with the photodetector allows a technique typically used in amplifier design known as gain peaking [24, 25] to be directly adapted to the silicon photonics platform. There are three variants that we describe. First, simple series gain peaking involves placing an inductor in series with the signal from the photodetector and the load; in this fashion, bandwidth can almost always be improved by around 40%. For a more advanced configuration involving a second capacitance, we show that improvements by as much as 100% are possible. Finally, for a technique we call shunt gain peaking, the maximum operating frequency can be increased by many times if narrow-band operation is acceptable.

Before specific gain peaking circuits can be discussed, however, the key parasitic value R_{pd} needs to be quantified. While detector capacitance is usually reported in the literature, R_{pd} is difficult to measure directly. If a geometry is known to not be transit-time limited, and the capacitance is known, then R_{pd} can be derived from the bandwidth using Eq. (1). For a typical value, consider the 35.2 fF, 2.3 μm x 64 μm detector studied in [19]; R_{pd} can be calculated to be 130 Ω.

2. Gain peaking enhanced photodetector circuits

2.1 Series gain peaking

Consider adding an inductor in series with the load of a photodetector, as shown in Fig. 3.
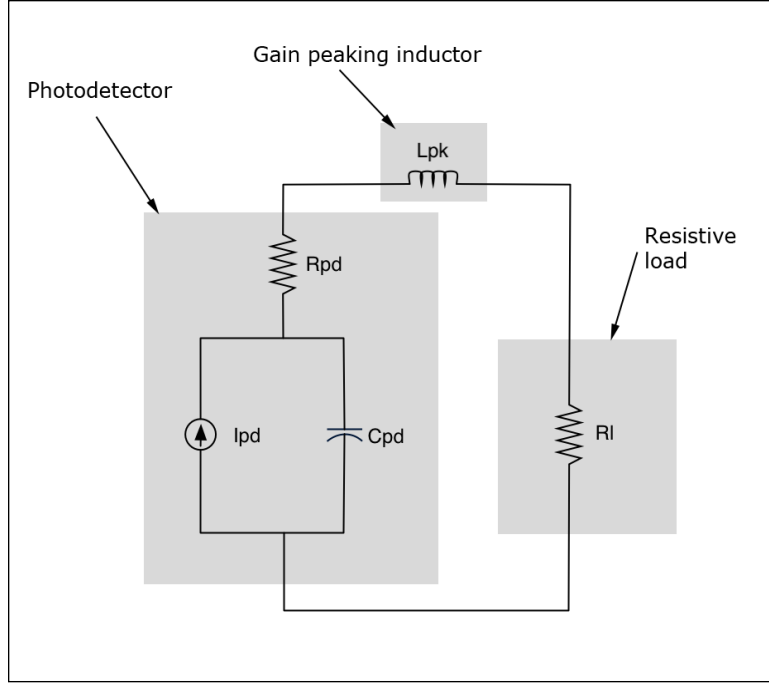
Fig. 3. Small-signal AC model of a series gain peaked photodetector circuit.

Here the new element L_{pk} is the gain peaking inductor. The bandwidth of this detector will no longer have the form shown in (1), but instead will have the form:

$$f_c = \frac{\sqrt{2}}{2\pi\left(R_L + R_{pd}\right)C_{pd}} \tag{2}$$

This will occur if the value of the inductor is chosen to be:

$$L_{pk} = \frac{C_{pd}\left(R_L + R_{pd}\right)^2}{2} \tag{3}$$

To take a concrete example, consider the previously described detector [19] with values C_{pd} of 35.2 fF and R_{pd} of 130Ω. For a 50Ω load the un-peaked bandwidth would be 25 GHz. The gain peaked bandwidth is 35.5 GHz. The inductance L_{pk} needed is 0.57 nH. We show the normalized responsivity, and phase shift of the photodetector circuit, in Fig. 4. Here phase shift refers to the AC phase shift between the current through the load resistance, and the current produced by the photodetector.
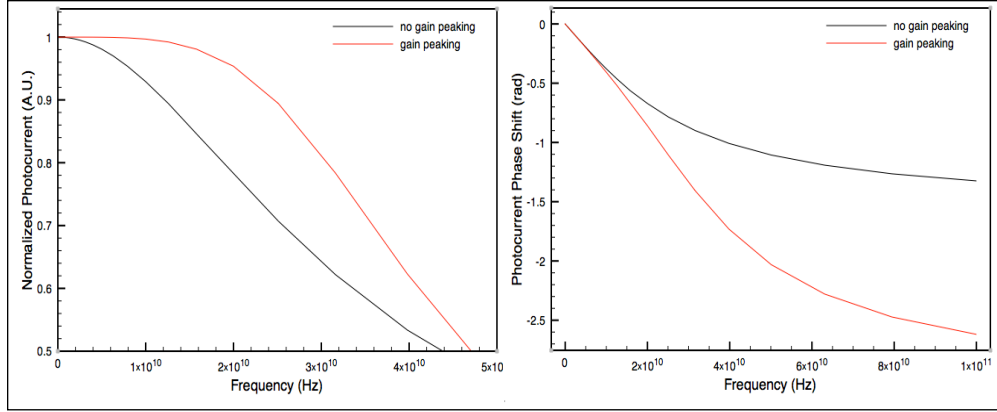
Fig. 4. Normalized responsivity and phase shift as a function of frequency for the series-peaked photodetector, using the circuit values Cpd=35.2 fF, Rpd=130Ω, Rl=50Ω and Lpk=0.57 nH. For comparison the un-peaked detector performance is shown (Lpk=0).

One key issue is that of dispersion; a deviation from a linear relation between the phase shift of the circuit and frequency implies a non-uniform time delay for different frequencies, which would distort signals. In this example, the maximum level of dispersion is 0.3 ps of excess delay for the frequency 30 GHz, which is a small fraction of the period of the 35.5 GHz bandwidth, and therefore is likely not an issue.

As we will discuss in a later section, the inductance value of 0.57 nH is plausible for an integrated inductor in the process described earlier. We note that this large bandwidth improvement is due to nothing more than a simple spiral inductor, which could be placed between one contact on the detector and 50-Ω contact pads for an externally coupled photodetector. Note that as long as the detector is not transit-time limited, a bandwidth enhancement of 40% is always possible, regardless of R_{pd}.

2.2 Enhanced series gain peaking

Consider adding a capacitor C_l to the circuit shown Fig. 3 in parallel with the load, as shown in Fig. 5. This could correspond to a parasitic capacitance due to bump bonding [21] or from another source. Traditionally this capacitance would be seen as an undesirable parasitic, and would have further degraded photodetector bandwidth; however, with the right choice of inductor, this capacitance can actually lead to enhanced performance. Therefore, it might also prove desirable to intentionally add this capacitance, perhaps with a MIM capacitor.
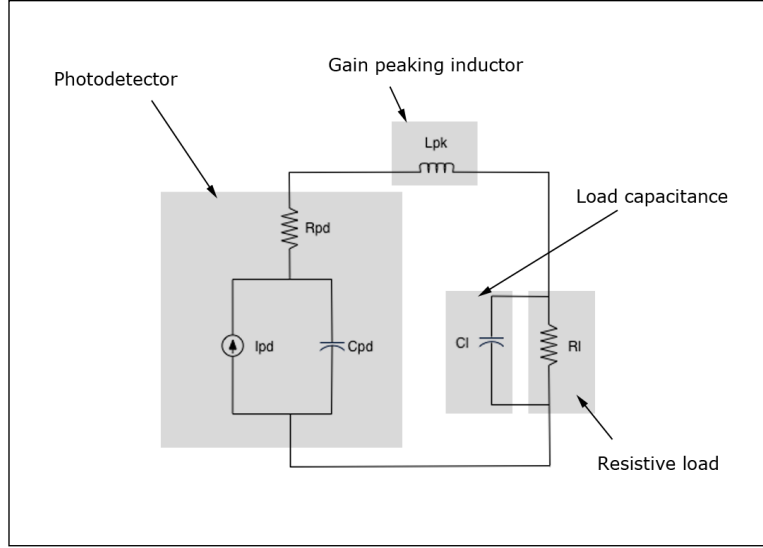
Fig. 5. Small-signal AC circuit for an enhanced series gain peaked photodetector circuit. The additional capacitor C_l is in parallel with the load resistance. This could be a load capacitance due to bump-bonding or another form of packaging, or it could be an intentionally added capacitance via a MIM capacitor layer.

Unfortunately, closed form expressions for the optimal choices of L_{pk} and C_l are not readily available to the authors; these values need to be solved for numerically. Significant enhancements can be obtained, though generally speaking R_l needs to be significantly larger than R_{pd} for 100% improvements in bandwidth to be approached. For many photodetectors R_{pd} is comparable or larger than R_l, and so further process development may be required to fully realize these bandwidth enhancements. Alternatively, higher load resistances can be used, though eventually the required inductances rise to a challenging level. Table 1 shows the optimal choices of C_l, L_{pk} in a number of situations, and the new cutoff frequency in an enhanced gain peaking circuit, f_c'.

Table 1. Some examples of enhanced gain peaking circuits, with the enhanced bandwidths compared to the original, un-peaked bandwidths.

Example	R_{pd} (Ω)	C_{pd} (fF)	R_l (Ω)	f_c (GHz)	L_{pk} (pH)	C_l (fF)	f_c' (GHz)	Improvement Percentage
1	25	100	50	21.2	375	100	31.8	50%
2	5	100	50	29	160	77	57	97%
3	25	100	300	4.9	5680	74	9.7	98%
4	130	32.5	600	6.7	9570	30.7	11.9	78%

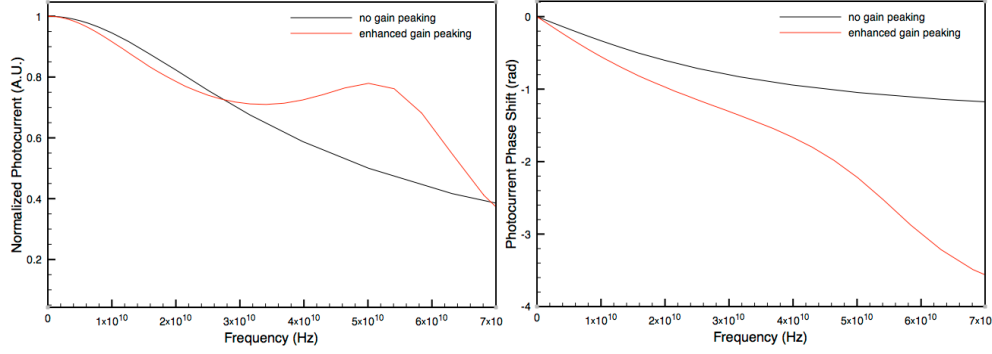The normal and enhanced gain peaked bandwidths are shown for example 2 in Fig. 6.

Fig. 6. Normal and enhanced series gain peaked photodetector circuit performance. Here $R_{pd}=5\Omega$, $C_{pd}=100fF$, $R_l=50\Omega$, $C_l=77fF$, $L_{pk}=160pH$.

In the case of Fig. 6, the maximum dispersion is around 0.6 ps of extra delay at 46 GHz, which is likely negligible.

2.3 Shunt peaking

It is well known that the performance of CMOS circuits, typically limited by gate capacitances, can be enhanced through inductance [24, 25]. In particular, circuits can be made narrow-band at frequencies well above the range at which broadband amplifiers can be constructed. The same idea can readily be applied to capacitance-limited photodetectors. Fig. 7 shows a detector circuit in what we call a shunt peaked configuration. Note than an extra blocking capacitor C_b is present, to prevent a short at low speed.
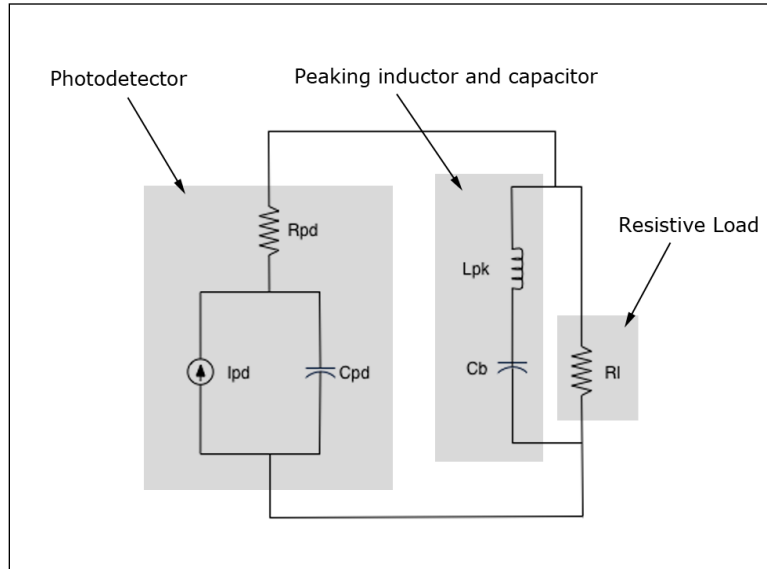

Fig. 7. Shunt peaking photodetector small-signal AC circuit.

Here, Rpd needs to be decreased substantially to fully realize the benefits of this geometry. But if this can be accomplished, operating frequencies of the shunt peaked detector can be extended to well beyond what could be achieved with even enhanced series peaking. For example, if C_{pd} = 100 fF, R_{pd} = 2 Ω, R_l = 50Ω, L_{pk} = 50 pH, and C_b = 1 pF, the shunt peaked photodetector will exhibit 82% of the DC responsivity at 73.4 GHz, with a 3 dB bandwidth of 34.3 GHz; that is, an operating window from 59.1 GHz to 93.4 GHz. The original, un-peaked bandwidth of this detector would be 30.6 GHz. Fig. 8 shows the normalized photocurrent and phase shift.
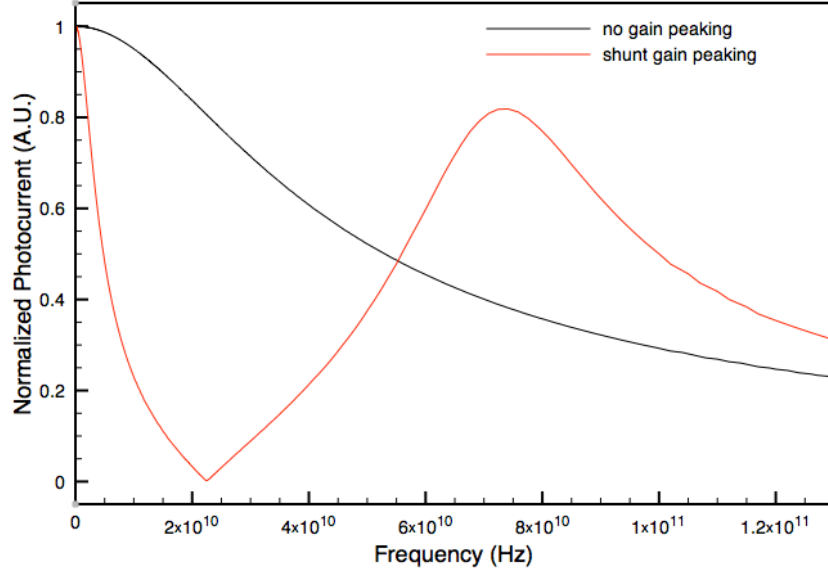

Fig. 8. Normalized photocurrent for the shunt peaked photodetector circuit. For comparison, the unpeaked detector circuit performance is also shown.

3. Inductor parasitics and noise sources

3.1 Inductor geometry and parasitics

Integrated inductors sometimes require large areas, and inevitably imply parasitic resistances, as well as self-capacitances. Fortunately, the typical inductance that would be needed for a gain peaking circuit can be easily realized with the geometry described in Fig. 2. Consider an inductor formed by a two-loop square spiral with 10 µm wide traces, as shown in Fig. 9. The outer loop traces a 65-µm square (center of the trace), while the inner loop traces a 50-µm square. The total area used for the inductor is a 75 µm x 75 µm square.
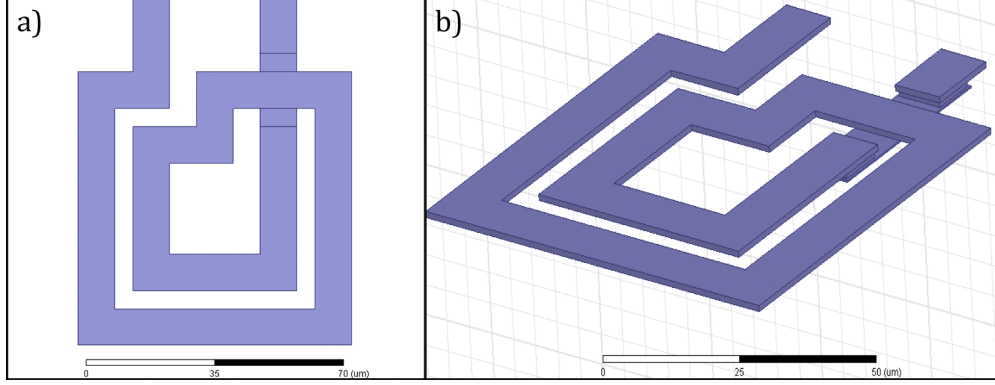
Fig. 9. Layout of example inductor with 290 pH inductance as viewed from above (a) and in isometric view (b). Only 75 x 75 um^2 is required.

The bulk of the inductor is made from the thicker top metal layer, while the lower metal layer is used for the metal crossing. A full 3-dimensional electromagnetic simulation of the inductor was performed using commercial software (HFSS from Ansys). The results show that the structure will have an inductance of 290 pH, a self-capacitance of 6 fF, and a series resistance of 0.6 $\Omega / \sqrt{GHz}$. The parasitic resistance and self-capacitance are both small fractions of the load and photodetector parasitics described in section 2.1; we can thus expect the parasitic values to have little impact on the performance of the photodetector circuit, at least for conventional gain peaking.

3.2 Noise analysis

Pure inductance and capacitance are considered noiseless, but the parasitic resistance in series with the inductor contributes thermal noise to the output. Using two-port analysis one can refer this contribution back to the input port, as a noise current in parallel with the photocurrent source for fair comparison between different circuit topologies [26].

It is straightforward to show that for series peaking and enhanced series peaking, the input-referred noise current spectrum density is

$$\overline{i_{in,n}^{2}} = 4kTR_{series}\omega^{2}C_{pd}^{2} \tag{4}$$

where k is the Boltzmann constant, T is the temperature of the circuit and R$_{series}$ is the series resistance of the inductor. As a comparison, the input-referred noise due to R$_{pd}$ is

$$\overline{i_{in,n}^{2}} = 4kTR_{pd}\omega^{2}C_{pd}^{2} \tag{5}$$

Therefore as long as R_{series} is small compared to R_{pd} within the operating frequency bandwidth, the series peaking technique does not introduce significant noise.

For shunt peaking, neglecting C_b, the input-referred noise due to R_{series} can be expressed as:

$$\overline{i}_{in,n}^2 = 4kTR_{series}\frac{1+\omega^2 C_{pd}^2 R_{pd}^2}{R_{series}^2 + \omega^2 L^2} \qquad (6)$$

The total output noise in the circuit illustrated in Figure 7 will have to include the noise contribution of the load [26]. Here we assume a 50 Ω resistive load, which is equivalent to assuming a TIA with 3dB noise figure or a 50 Ω terminated transmission line. This load exhibits a noise current of

$$\overline{i}_{in,n}^2 = 4kT\frac{1+\omega^2 C_{pd}^2 R_{pd}^2}{R_L} \qquad (7)$$

when referred to the input. The ratio of the excess noise introduced by shunt peaking to the noise from the load is thus:

$$\frac{R_{series}}{R_L\left(R_{series}^2 + \omega^2 L^2\right)} \qquad (8)$$

Using the parameters in the shunt peaking example near mid-band, at 80GHz this ratio is 0.4. It is important to note that in addition to thermal noise a, typical optical receiver end also suffers from shot noise and relative laser intensity noise, which are usually the dominating factor in the normal operation regime of a photodetector [27]. It can be shown that the shot noise will be as large as the total thermal noise from various sources in the shunt peaking circuit when the photocurrent is 1.4 mA. Therefore for photodetectors operating with this level of current or higher, the shunt peaking technique has an increasingly small impact on the overall noise performance.

4. Conclusions

We have shown that using properly chosen inductors, it is always possible to improve the bandwidth of a capacitance-limited photodetector by at least 40%. All that is required are two metal layers. A large number of photodetectors reported in the literature could likely have their performance improved through the use of this technique. It is also possible in some circumstances to increase the bandwidth even beyond this value if the parasitic resistance of the photodetector is low. We believe that future silicon photonics detectors should leverage the complexity available in the CMOS compatible silicon photonics platform to improve performance in this fashion.

Inductive Peaking Photodetector experimental demonstration:

Our MPW wafers were fabricated at the Institute of Microelectronics (IME)/ASTAR [5]. The process starts with 8" Silicon-on-Insulator (SOI) wafer from SOITEC with 220nm top silicon and 2um bottom oxide thickness. 750Ω.cm high resistivity handle silicon was used to ensure the RF performance. A 60 nm anisotropic dry etch was first applied to define the grating couplers. Next, silicon rib and channel waveguides were formed using 2 additional etch steps. The p++, p+, p, n++ ,n+ and n implants for the Si modulator and the p-type doping for anode formation of the Ge p-i-n photodetectors were performed on the exposed silicon, prior to any oxide fill. This was followed by a rapid thermal anneal at 1030 ºC for 5 s for Si dopant activation. Ge was then selectively grown to a thickness of 500 nm in regions defined by a deposited SiO_2 mask layer. Ion implantation was performed for the Ge regions and annealed at 500 ºC for 5 min, followed by the formation of contact vias and two levels of aluminum interconnects. Chemical-mechanical planarization (CMP) was not utilized. The schematic cross-section is shown in Fig 1 below.
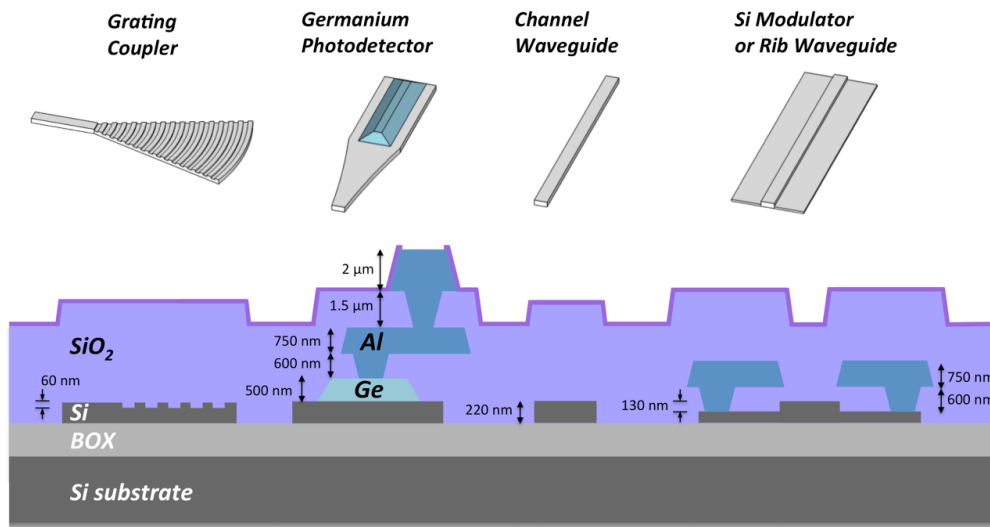

Illustration of the cross-section of opsis platform[6]

Photodetectors (PD) were constructed with vertical Germanium p-i-n diodes. A spiral metal inductor in series with the diode was employed to improve the bandwidth [7]. An average responsivity of 0.7A/W was achieved at 2V reverse bias, with 5uA dark current. To character the RF performance of the detector, we used a vector network analyzer (VNA) to drive a high-speed Lithium Niobate (LiNbO3) modulator, and detect the electrical output from the PD. The EO response of the modulator was calibrated by an ultrafast commercial photodetector whose bandwidth was larger than 70GHz, and was normalized out in our PD measurement. Using this methodology, the 3dB bandwidth of our PD is measured to be 58GHz when 2V reverse bias was applied as shown in figure 2.
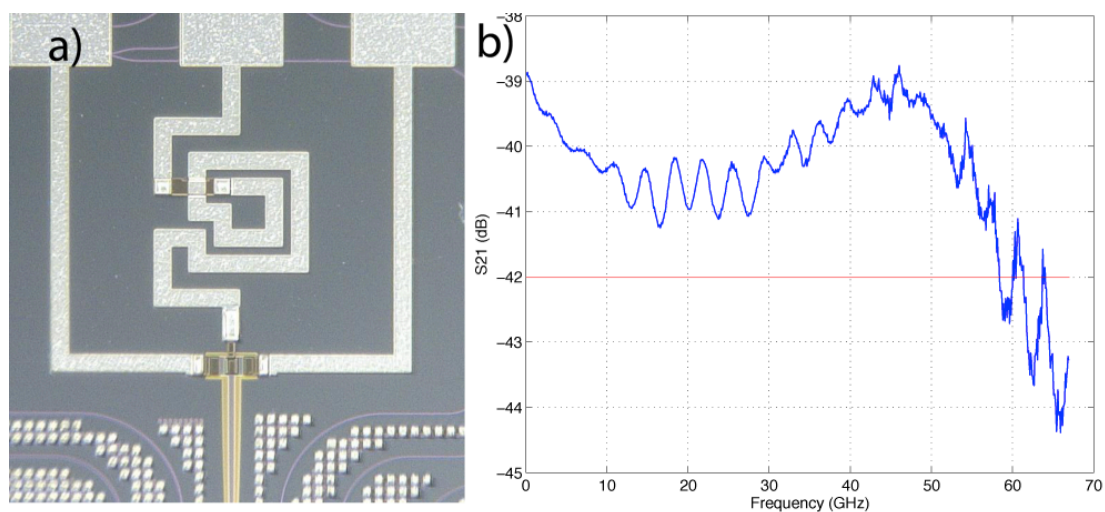

Fig 2 a: Image of inductive peaking PD. b: EO response of inductive peaking PD, 58GHz bandwidth was achieved.

Commercialization activity:

Portage Bay Photonics:

Purpose:

Portage Bay Photonics is the commercialization arm of the Nanophotonics group. It was set up to receive STTR monies and commercialize nanophotonic devices that were developed by the Nanophotonics lab and licensed by the UW. It has been set up as a for profit corporation. Portage Bay Photonics, PBP, is a Delaware corporation doing business in Newark DE, This organization is now the recipient of two STTR grants. In addition, we anticipate significant further commercial activity in the coming year.

Strategic integration:

Concepts and ideas will be conceived and prototyped out of the Nanophotonics group. Patents will be held by the UW and licensed to Portage Bay Photonics for commercialization. Portage Bay is a for profit company.   PBP has completed license agreement to the relevant UW IP and are now negotiating with UD.